LH543611/21

FEATURES

- Fast Cycle Times: 20/25/30/35 ns
- Pin-Compatible, Deeper 0.7μ-Technology Replacements for Sharp LH5420 and LH543601
- Functionally Upwards-Compatible from LH5420 and LH543601
- Two 512 × 36-bit or 1024 × 36-bit FIFO Buffers
- Full 36-bit Word Width
- Selectable 36/18/9-bit Word Width on Port B; Selection May be Changed Without Resetting the BiFIFO
- Programmable Byte-Order Reversal – 'Big-Endian ↔ Little-Endian Conversion'
- Independently-Synchronized ('Fully-Asynchronous') Operation of Port A and Port B
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- R/W̅, Enable, Request, and Address Control Inputs are Sampled on the Rising Clock Edge
- Synchronous Request/Acknowledge 'Handshake' Capability; Use is Optional
- Device Comes Up Into a Known Default State at Reset; Programming is Allowed, but is not Required
- Asynchronous Output Enables
- Five Status Flags per Port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- All Flags are Independently Programmable for Either Synchronous or Asynchronous Operation
- Almost-Full Flag and Almost-Empty Flag Have Programmable Offsets
- Mailbox Registers with Synchronized Flags
- Data-Bypass Function
- Data-Retransmit Function
- Automatic Byte Parity Checking
- Programmable Byte Parity Generation
- Programmable Byte-Oriented or Halfword-Oriented Parity Operations
- 8 mA-I_{OL} High-Drive Three-State Outputs with Built-In Series Resistor
- TTL/CMOS-Compatible I/O
- Space-Saving PQFP and TQFP Packages
- PQFP to PGA Package Conversion *

FUNCTIONAL DESCRIPTION

The LH543611/21 contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bidirectional data buffering. FIFO #1 and FIFO #2 each are organized as 512/1024 by 36 bits. The LH543611/21 is ideal either for wide unidirectional applications or for bidirectional data applications; component count and board area are reduced.

The LH543611/21 has two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals.

An eighteen-bit Control-Register governs the synchronization mode of the fullness-status flags at each port, the choice of odd or even parity at both ports, the enabling of parity generation for data flow at each port, the optional latching behavior of the parity-error flags at each port, and the selection of a full-word or half-word or single-byte field for parity checking. A reset operation initializes the LH543611/21 Control Register for LH5420/LH543601-compatible operation, but it may be reprogrammed at will at any time during LH543611/21 operation.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for *each* FIFO. Each of these flags may be independently programmed for either synchronous or asynchronous operation. Also, the Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 512/1024 or fewer words may be retransmitted any desired number of times.

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a New-Mail-Alert Flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can

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*   For PQFP-to-PGA conversion for hru-hole board designs, Sharp recommends ITT Pomona Electronics' SMT/PGA Generic Converter model #5853.® This converter maps the LH543611/21 132-pin PQFP to a generic 13 × 13, 132-pin PGA (100-mil pitch). For more information, contact Sharp or ITT Pomona Electronics at 1500 East Ninth Street, Pomona, CA 91766, (909) 469-2900.

BOLD = Improved or added features over SHARP's LH5420 architecture/feature set.

FUNCTIONAL DESCRIPTION (cont'd)

use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths. Subject to meeting timing requirements, the word-width selection may be changed at any time during the operation of an LH543611 or LH543621, without the need either for a reset operation or for passing

dummy words through Port B immediately after the change.

A Byte Parity Check Flag at each port monitors data integrity. Control-Register bit 0 (zero) selects the parity mode, odd or even. This bit is initialized for odd data parity at reset; but it may be reprogrammed for even parity, or back again to odd parity, as desired. The parity flags may be programmed to operate in either a latched mode or a flow-through mode.

Parity generation, when selected, creates the parity bit of each 8-bit byte of the input word. The result is written into the MSB-bit of each 9-bit byte, overwriting the previous contents of the bit.
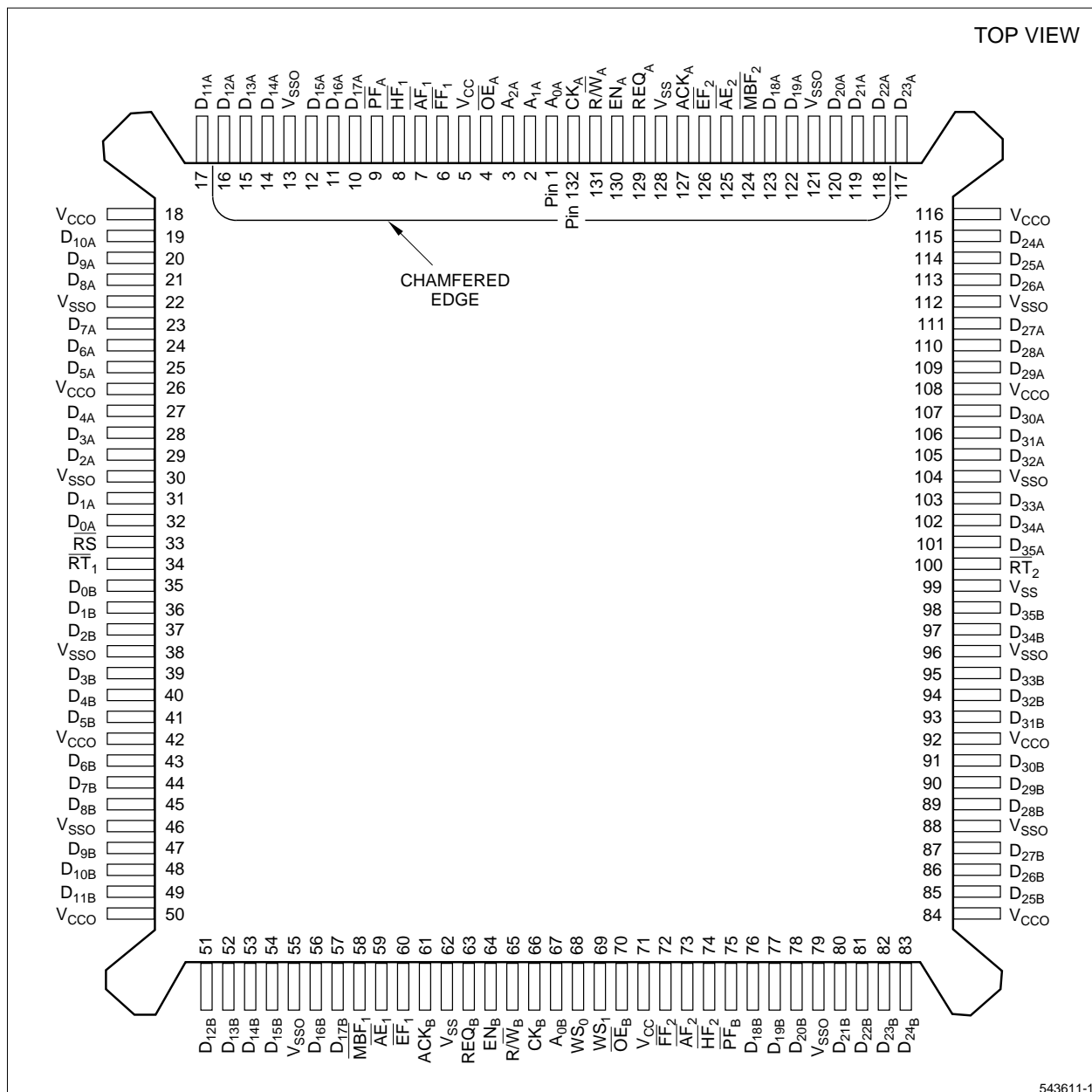
PIN CONNECTIONS

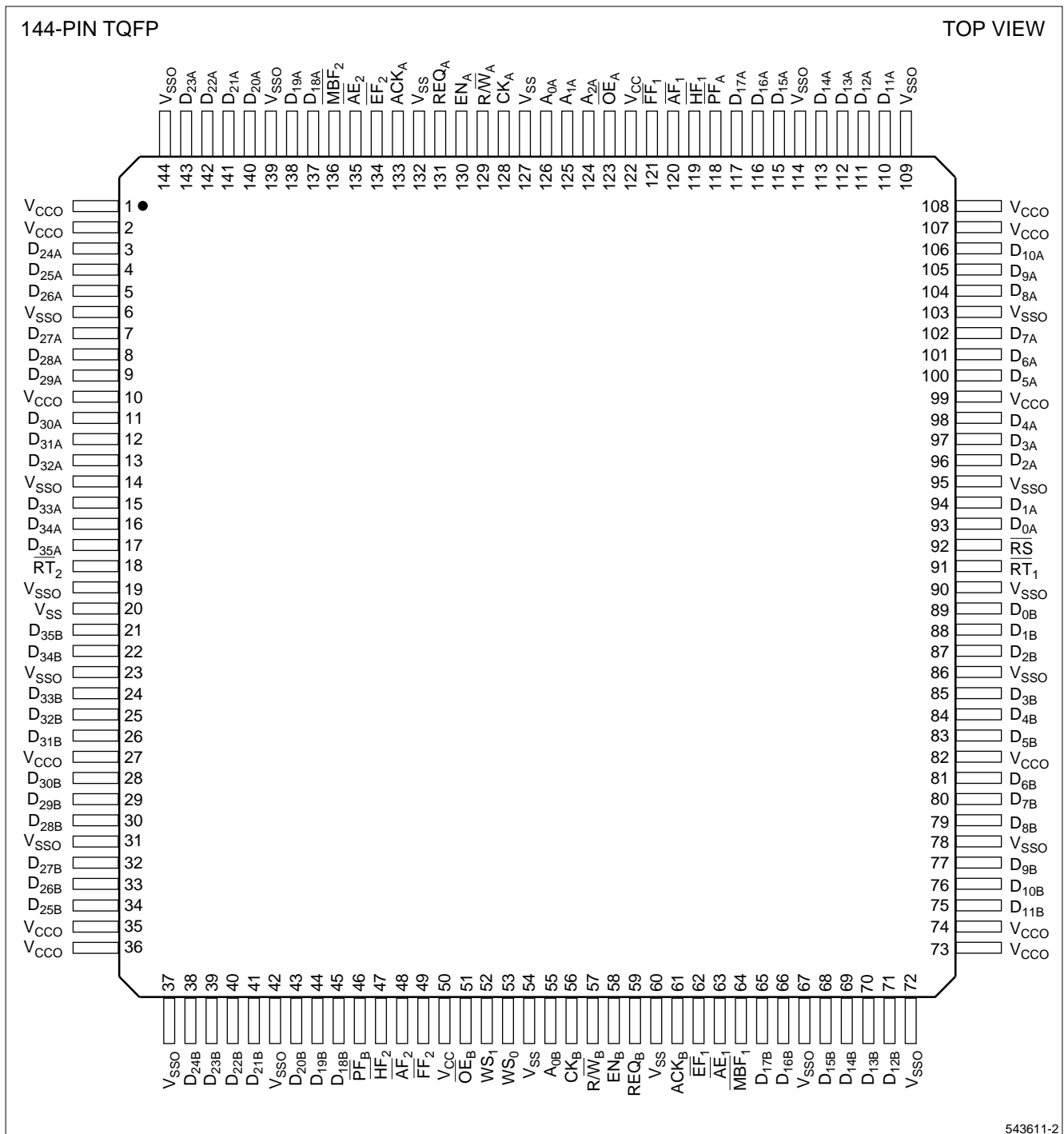**Figure 1. Pin Connections for 132-Pin PQFP Package (Top View)**

144-PIN TQFP   TOP VIEW
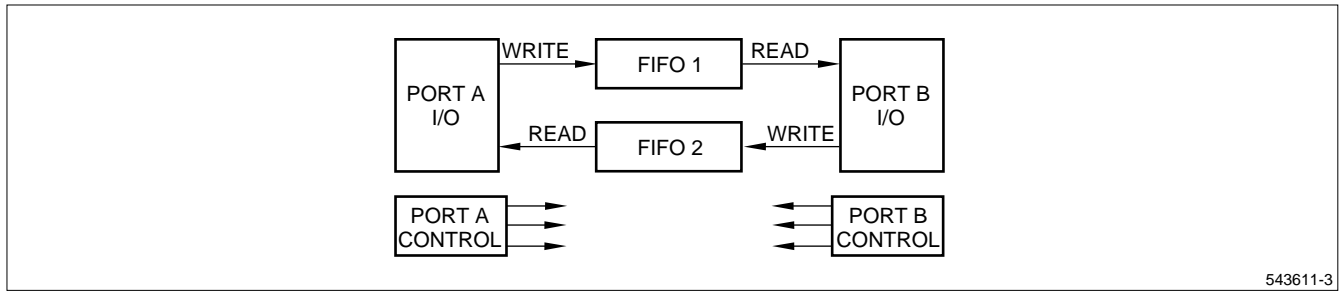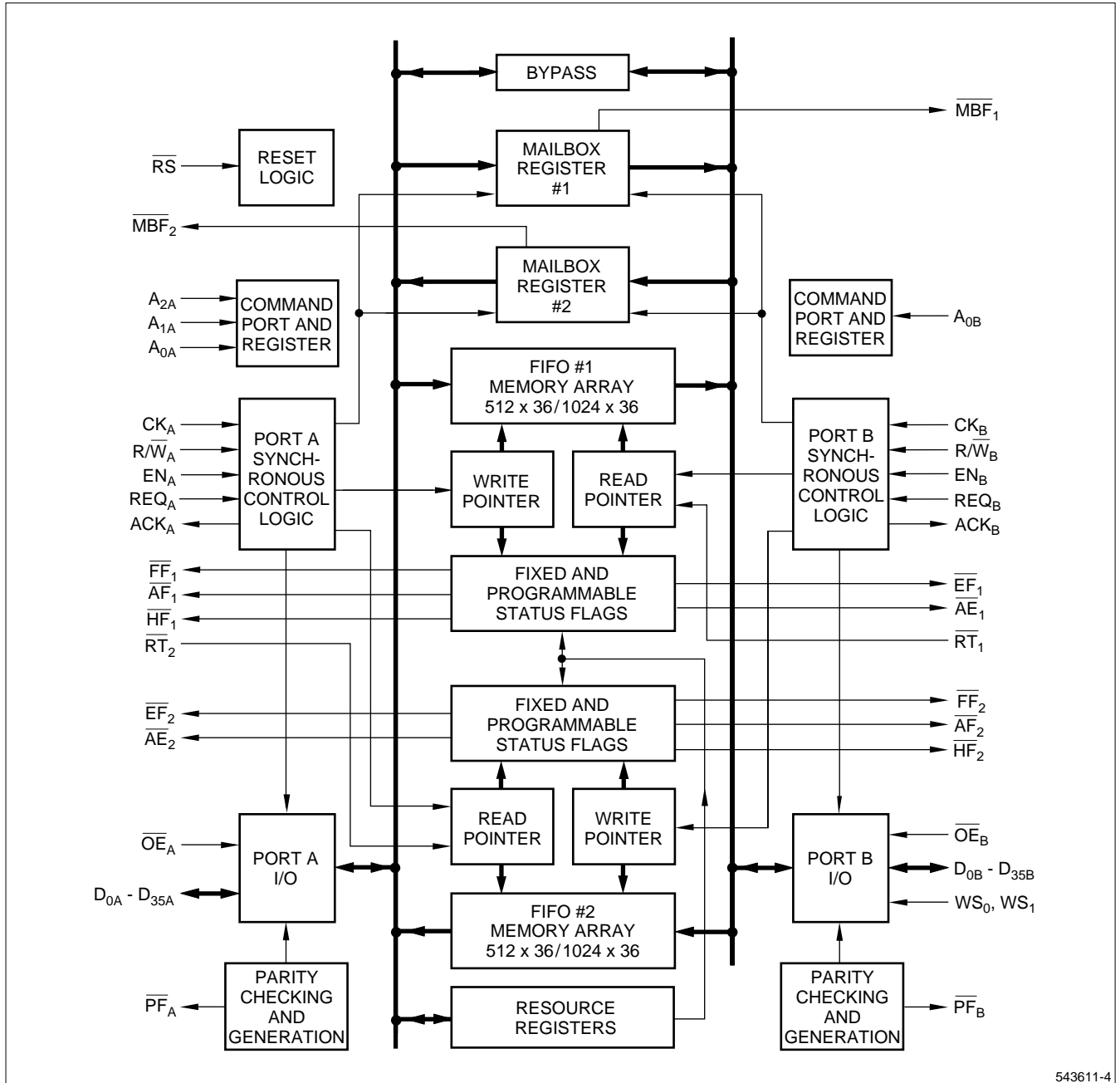

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Figure 2. Pin Connections for 144-Pin TQFP Package
(Top View)

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Figure 3a. Simplified LH543611 Block Diagram

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Figure 3b. Detailed LH543611 Block Diagram

Table 1. Control-Register Format

PORT	COMMAND REGISTER BITS	CODE	VALUE AFTER RESET	FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
A, B	00	L	H	$\overline{PF_A}$, $\overline{PF_B}$	EVEN parity in effect.	A correct 9-bit byte has an even number of ones.
		H			ODD parity in effect.	A correct 9-bit byte has an odd number of ones.
A	01	L	L	–	Disable Port A parity generation.	No overwriting of parity bits.
		H			Disable Port A parity generation.	Parity bit over eight least-significant bits of each byte is overwritten into the most-significant bit of that byte.
	02	L	L	$\overline{PF_A}$	Port A parity-error flag operates 'flow-through.'	$\overline{PF_A}$ is subject to transient glitches while data bus is changing.
		H			Port A parity-error flag is latched by CK_A.	$\overline{PF_A}$ remains steady until its value should change.
	03	L	L	$\overline{EF_2}$	Set by $\uparrow CK_A$, reset by $\uparrow CK_B$.	Asynchronous flag clocking.
		H			Set and reset by $\uparrow CK_A$.	Synchronous flag clocking.
	04	L	L	$\overline{AE_2}$	Set by $\uparrow CK_A$, reset by $\uparrow CK_B$.	Asynchronous flag clocking.
		H			Set and reset by $\uparrow CK_A$.	Synchronous flag clocking.
	06, 05	LL	LL	$\overline{HF_1}$	Set by $\uparrow CK_A$, reset by $\uparrow CK_B$.	Asynchronous flag clocking.
		LH			Set and reset by $\uparrow CK_B$.	Synchronous flag clocking by Port B clock.
		HL, HH			Set and reset by $\uparrow CK_A$.	Synchronous flag clocking by Port A clock.
	07	L	L	$\overline{AF_1}$	Set by $\uparrow CK_A$, reset by $\uparrow CK_B$.	Asynchronous flag clocking.
		H			Set and reset by $\uparrow CK_A$.	Synchronous flag clocking.
	08	L	L	$\overline{FF_1}$	Set by $\uparrow CK_A$, reset by $\uparrow CK_B$.	Asynchronous flag clocking.
		H			Set and reset by $\uparrow CK_A$.	Synchronous flag clocking.
B	09	L	L	$\overline{PF_B}$	Parity check computed over all four bytes of each word.	Full-word parity-error indication regardless of $WS_1 - WS_0$ setting.
		H			Parity check computed over half-word or single-byte according to $WS_1 - WS_0$ setting.	Full-word, half-word, or single-byte parity-error indication according to $WS_1 - WS_0$ setting.
	10	L	L	–	Disable Port B parity generation.	No overwriting of parity bits.
		H			Enable Port B parity generation.	Parity bit over eight least-significant bits of each byte is overwritten into the most-significant bit of that byte.
	11	L	L	$\overline{PF_B}$	Port B parity-error flag operates 'flow-through.'	$\overline{PF_B}$ is subject to transient glitches while data bus is changing.
		H			Port B parity-error flag is latched by CK_B.	$\overline{PF_B}$ remains steady until its value should change.
	12	L	L	$\overline{EF_1}$	Set by $\uparrow CK_B$, reset by $\uparrow CK_A$.	Asynchronous flag clocking.
		H			Set and reset by $\uparrow CK_B$.	Synchronous flag clocking.

Table 1. Control-Register Format (cont'd)

PORT	COMMAND REGISTER BITS	CODE	VALUE AFTER RESET	FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
B	13	L	L	$\overline{AE}_1$	Set by ↑ CK$_B$, reset by ↑ CK$_A$.	Asynchronous flag clocking.
		H			Set and reset by ↑ CK$_B$.	Synchronous flag clocking.
	15, 14	LL	LL	$\overline{HF}_2$	Set by ↑ CK$_B$, reset by ↑ CK$_A$.	Asynchronous flag clocking.
		LH			Set and reset by ↑ CK$_A$.	Synchronous flag clocking by Port A clock.
		HL, HH			Set and reset by ↑ CK$_B$.	Synchronous flag clocking by Port B clock.
	16	L	L	$\overline{AF}_2$	Set by ↑ CK$_B$, reset by ↑ CK$_A$.	Asynchronous flag clocking.
		H			Set and reset by ↑ CK$_B$.	Synchronous flag clocking.
	17	L	L	$\overline{FF}_2$	Set by ↑ CK$_B$, reset by ↑ CK$_A$.	Asynchronous flag clocking.
		H			Set and reset by ↑ CK$_B$.	Synchronous flag clocking.

Table 2. Controllable Functions

TYPE	DESCRIPTION	CONTROL-REGISTER BIT	
		PORT A	PORT B
Parity	Even/Odd	0 [1]	0 [1]
	Policy for 9/18-Bit Word-Width Selection	–	9
	Generation: Enable/Disable	1	10
	Flag Behavior: Latched/Flowthrough	2	11
Flag Synchronization	$\overline{EF}$ Synchronous/Asynchronous	3	12
	$\overline{AE}$ Synchronous/Asynchronous	4	13
	$\overline{HF}$ Synchronous-With-Write/Synchronous-With-Read	5-6	14-15
	$\overline{AF}$ Synchronous/Asynchronous	7	16
	$\overline{FF}$ Synchronous/Asynchronous	8	17

NOTE:
1. LH5420/LH543601 also have this Control-Register function. Same Control-Register bit controls both Port A and Port B functionality.
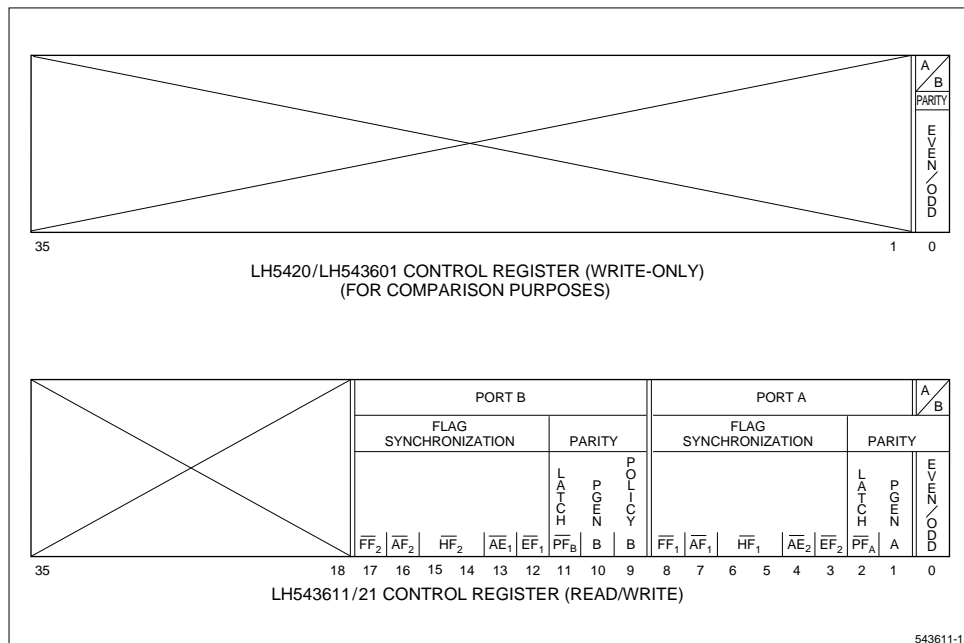

**Figure 4. LH5420/LH543601, and LH543611/21
Control-Register Formats**